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Nanometer scale gaps for capacitive transduction improvement on RF-MEMS resonators

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Abstract

In this work, we describe a simple 3-mask fabrication process, that allows us to prototype thick silicon lateral bulk acoustical resonators with nanometer scale transducing gaps. The vibrating parts of the MEMS resonator are fabricated on crystalline silicon, and the electrodes for lateral electrostatically excitation and detection are made with deposited polysilicon. The process is specially optimized to prevent overlapping of the polysilicon electrodes with crystalline moving parts, in order to avoid the excitation of vertical vibrating modes. Structures consisting on well known circular and ellipsoidal shape resonators have been designed using FEM simulations and fabricated in order to test the fabrication process. Detailed SEM images of some of the fabricated test structures, as well as the electrical characterization of their frequency response are reported.

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1. Introduction

It has been demonstrated that the introduction of radiofrequency vibrating MEMS as integrated components into transceiver architectures, can produce a revolutionary impact on the future generation of wireless communication systems. Such a so called RF-MEMS elements – mainly filters, switches, voltage-controlled oscillators and mixersgive significant advantages in terms of cost, size, frequency stability, phase noise, tunnability and power consumption; when compared to traditionally electronic implementations [1]. The operation principle of this kind of MEMS is based on the electrostatic excitation and the capacitive detection of both flexural and bulk longitudinal vibration modes of a mechanical resonating structure, by means of closely parallel placed electrodes. One of the most optimized configuration consists on applying an ac voltage to the excitation

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electrode (input port), a dc voltage directly to the resonator moving part, and then detecting the current signal that will be induced by the dc voltage at the resonator-output electrode capacitance (output port) [2].

In order to improve the capacitive transduction of such MEMS elements, one of the main issues is the quality factor of the mechanical resonator (Q). But, also coupling parameters as the area or the gap spacing of the transducing capacitances, which are more directly related to the layout, play an important role on the final optimization of the RF-MEMS performance. From the resonator shape design point of view, researchers have explored different structures in order to achieve high quality factors and adequate coupling parameters. Structures like beams, squares and circles have been extendedly reported [3–5]. From the fabrication technology perspective, also several fabrication strategies based on high mechanical performance materials have been explored to obtain MEMS with optimum parameters [8–10].

However, during the development of these RF-MEMS elements, a fast prototyping method based on a simple fabrication process is needed to explore new geometries or

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transduction strategies. Although some cheap procedures for a rapid prototyping have been previously reported [6,7], nanometer scale transducing gaps have not been reproducibly obtained.

In the present work, we propose a fabrication method based on the use of a sacrificial silicon oxide spacer for the transducing gap definition, that can be used as a parallel fast prototyping tool of RF-MEMS resonating elements. The fabrication process is based on only 3-mask levels to define the crystalline silicon resonating structures and their supporting mechanical anchors, and the polysilicon excitation and detection capacitive electrodes.

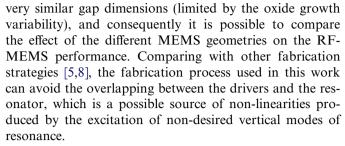
2. Fabrication process

In the fabrication process presented here, we have tried to maintain the CMOS compatibility in all the fabrication steps, avoiding the use of non compatible metals, like gold or platinum, and non-compatible lithographic processes. We have used SOI (silicon on insulator) wafers, 5 μ m thick in silicon and 2 μ m thick in silicon oxide. Silicon was p-type dopped.

The process is outlined in Fig. 1. Three lithographic steps are required, two RIE processes, three steps of aluminium deposition and one for polysilicon deposition and, finally, one etching to release the structure.

First, just at the place where the gap will be, a $2 \mu m$ width and $5 \mu m$ depth trenches are opened via RIE process. The next step is the oxidation of silicon, which will determine de gap width. In our case, it was performed an oxidation of around 60 nm in thickness. A polysilicon layer is then deposited in order to refill the trench and, at the same time, to use this polysilicon to define the pads of the total device circuit. It is necessary to make another photolithographic step to define the pads and to eliminate the excess of polysilicon above the structure and at the gap zones. Another photolithographic and a RIE step is needed to define the entire MEMS structure, engraving 5 μm thick of silicon layer. Finally, an etch with HF allows us to release the structure.

This fabrication method takes the advantage of batch parallel processes, from the fact that it is suitable for building a broad number of geometries, like beams, circles, squares and so on. Besides, all the MEMS structures have



There are some difficulties in this fabrication process. One of the most important problems is at the trench step. When the RIE etching arrives at the bottom of the trench, it is possible that the anisotropy of the attack could be degraded, producing a widening effect which can affect the geometry of the structure and the coupling with the driver, diminishing the quality factor and the capacitive readout transduction. With an accurate RIE process (time of the reaction and recipe well controlled) we can avoid this problem.

3. Design of the test structures

To decide which kind of structure is suitable to be fabricated, firstly, with a determined resonant frequency as a target and with an analytical solution for resonant modes (if the geometry of the resonator permits this analytical solution) we search the geometric parameters of the MEMS (for example, for a circle we can calculate the radius). The entire structure is not only the resonator as well, but is the resonator with their anchors and another kind of influences from the environment. These influences can affect the frequency of resonance (also the coupling parameters and quality factor). To take into account the effects due to the entire structure it is very suitable to perform FEM (finite element method) simulations, not only to take into account the influences of the issues mentioned above, but also to know at which kind of modes correspond the resonance frequencies of the device. For this purpose, we have used the commercial software, CoventorWare [11].

In Fig. 2, some examples of the designed structures are shown. We can see the aspect of the mode movement (following the movement grade) and the corresponding resonant frequency. Generally, the anchors are the main path for the MEMS energy dissipation and quality factor reduction of the device. It is very difficult to predict the amount

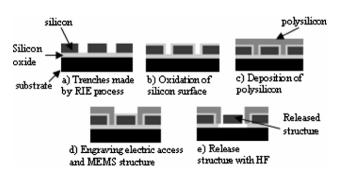


Fig. 1. Fabrication process scheme.

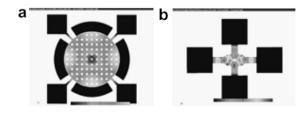


Fig. 2. Two examples of FEM simulations made by CoventorWare software. (a) circle with $27.9 \,\mu$ m radius and 100 MHz theoretical resonance, and (b) ellipse with 10.2 μ m major semiaxis and 5 μ m minor semiaxis with 417 MHz of resonance frequency.

of energy dissipated through the anchors, but it is possible to compare different configurations of the device to choose the better for quality factor purposes. For example, FEM simulations allow us to design the best places to put the anchor arms and the geometry of these arms.

4. Electrical characterization of test structures

Following the fabrication process mentioned above, and with the previous design studies and FEM simulations, we have fabricated some devices, with different geometries, to test which one of these structures are the most suitable for obtain a good MEMS. We have made beams, circles, squares and ellipses following the same fabrication method, which is useful for a wide range of geometries.

In Fig. 3, we can see two examples of fabricated devices, corresponding to the designs shown in Fig. 2. We can see a detail of the gap, below 100 nm.

We have used the two port configuration for electrical characterization, in which the MEMS is excited with an ac voltage in order to drive it to resonance plus a dc voltage to generate a measurable current at resonance, both applied at the same driver (through a bias-tee). This current was measured by means of a network analyzer and without any kind of amplification.

In Fig. 4, we can see S_{21} magnitude measurements in which the peaks corresponding to the MEMS resonance are clearly shown. There is a good agreement between the position of these peaks and the resonant frequencies calculated by FEM simulations. Due to the fact that the S_{21} measurements were made without any kind of signal amplification, the magnitude of the peaks are poor, but enough to be detected. For this reason, it is very difficult to calculate the Q factor, for which it is necessary to have a large peak in magnitude. It is possible that Q factor is not good enough in the present results (the peaks are broad in frequency scale). There are many factors that can affect Q factor, as for example, the existence of remainder oxide at the gap (due to its reduced width, it is difficult for the liquid HF solution to penetrate into the gap), the artificial holes of the structure (made for release reasons) or some defects introduced during the fabrication process. The optimization of the Q factor (trying to improve the fabrication steps or the release process) is being in research process.

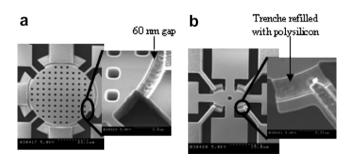


Fig. 3. SEM images of the fabricated devices corresponding to the circle and ellipse design of Fig. 2.

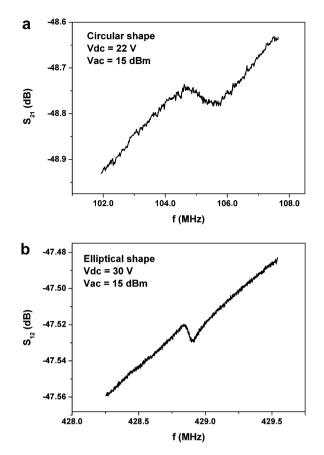


Fig. 4. Frequency response of the transmission S_{21} parameter measured for the circle (a) and ellipse (b) of Fig. 3.

5. Conclusions

In this work, we have presented a 3-mask fabrication process which allows us to prototype MEMS with a lateral gap below 100 nm wide for capacitive coupling readout purposes. This fabrication process is compatible with a great amount of geometric configurations, not only for the MEMS but for the electrical configuration as well and also compatible with CMOS processes.

MEMS fabricated with this process can be measured without any kind of amplification, which simplifies device architecture. With the described process it will be possible to fabricate MEMS at the UHF range, not far from 1 GHz modal frequencies with nanogaps for transducing signals.

Acknowledgement

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